LISTING OF CLAIMS:

This Listing of Claims, as presently pending, is provided for convenient reference:

1. (Previously presented)   Computer-readable media tangibly embodying a key-caching program executable on a computer and operating on a packet received from an external source, the computer including a system memory and a cache, the system memory and the cache including entries for source addresses and corresponding keys, the packet including a header that is not encrypted and a body that is encrypted, the key-caching program comprising code for:

establishing acknowledgment-responsive wireless communication with the external source;

extracting from the header a source address;

determining whether the source address is included in an entry in the cache;

when the source address is included in an entry of the cache, authorizing an acknowledgment signal for the external source, extracting from the entry of the cache a key corresponding to the source address, and using the key to decrypt the body of the packet;

when the source address is not included in an entry of the cache, determining whether the source address is included in an entry of the system memory; and

when the source address is not included in an entry of the cache and the source address is included in an entry of the system memory, extracting from the entry of the system memory a key corresponding to the source address, and storing the source address and the key as a new entry in the cache to prepare the cache for decrypting a packet subsequently re-sent by the external source.

2. (Original) Computer-readable media as claimed in claim 1, wherein the key-caching program further comprises code to effect:

when the source address is not included in an entry of the cache, dropping the packet.

3. (Previously presented) Computer-readable media as claimed in claim 1, wherein the key-caching program further comprises code to effect:

when the source address is not included in an entry of the cache, authorizing an acknowledgment signal for anticipatory transmission to the external source of the packet prior to retrieval of the key corresponding to the source address; and

when the source address is not included in an entry of the cache and the source address is included in an entry of the system memory, using the key to decrypt the body of the packet prior to arrival of a subsequent packet from the external source.

4. (Original) Computer-readable media as claimed in claim 1, wherein the cache includes fast memory.

5. (Original) Computer-readable media as claimed in claim 2, wherein the cache includes fast memory.

6. (Original) Computer-readable media as claimed in claim 3, wherein the cache includes fast memory.

7. (Previously presented) A key-caching system for operation on a packet received from an external source, the packet comprising a header that is not encrypted and a body that is encrypted, the key-caching system comprising:

a system memory,

a networking unit, the networking unit including a cache, the system memory and the cache including entries for source addresses and corresponding keys,

MR2919-18
Serial Number: 09/662,991
Reply to Office Action dated 14 June 2006

a processor, the system memory including a key-caching program

that is executable on the processor, and

a controller, the controller effecting communication and data transfer

between the system memory, the networking unit and the processor, wherein the

key-caching program comprising code to effect:

establishing acknowledgment-responsive wireless

communication with the external source;

extracting from the header a source address;

determining whether the source address is included in an

entry in the cache;

when the source address is included in an entry of the cache,

authorizing an acknowledgment signal for the external source, extracting from the

entry of the cache a key corresponding to the source address, and using the key to

decrypt the body of the packet;

when the source address is not included in an entry of the

cache, determining whether the source address is included in an entry of the

system memory; and

when the source address is not included in an entry of the

cache and the source address is included in an entry of the system memory,

extracting from the entry of the system memory a key corresponding to the source

address, and storing the source address and the key as a new entry in the cache to

prepare the cache for decrypting a packet subsequently re-sent by the external source.

8. (Original) A key-caching system as claimed in claim 7, wherein the key-caching program further comprises code to effect:

when the source address is not included in an entry of the cache, dropping the packet.

9. (Previously presented) A key-caching system as claimed in claim 7, wherein the key-caching program further comprises code to effect:

when the source address is not included in an entry of the cache, authorizing an acknowledgment signal for anticipatory transmission to the external source of the packet prior to retrieval of the key corresponding to the source address; and

when the source address is not included in an entry of the cache and the source address is included in an entry of the system memory, using the key to decrypt the body of the packet prior to arrival of a subsequent packet from the external source.

10. (Original) A key-caching system as claimed in claim 7, wherein the cache includes fast memory.

MR2919-18
Serial Number: 09/662,991
Reply to Office Action dated 14 June 2006

11. (Original) A key-caching system as claimed in claim 8, wherein the cache includes fast memory.

12. (Original) A key-caching system as claimed in claim 9, wherein the cache includes fast memory.

13. (Previously presented) A method of key caching with a system memory and a cache, the system memory and the cache including entries for source addresses and corresponding keys, the method comprising:

establishing acknowledgment-responsive wireless communication with an external source;

receiving a packet from the external source, the packet including a header that is not encrypted and a body that is encrypted;

extracting from the header a source address;

determining whether the source address is included in an entry in the cache, authorizing an acknowledgment signal for the external source, extracting from the entry of the cache a key corresponding to the source address, and using the key to decrypt the body of the packet;

when the source address is not included in an entry of the cache, determining whether the source address is included in an entry of the system memory; and

when the source address is not included in an entry of the cache and the source address is included in an entry of the system memory, extracting from the entry of the system memory a key corresponding to the source address, and storing the source address and the key as a new entry in the cache to prepare the cache for decrypting a packet subsequently re-sent by the external source.

14.   (Original) A method of key caching as claimed in claim 13, further comprising:

when the source address is not included in an entry of the cache, dropping the packet.

15.   (Previously presented) A method of key caching as claimed in claim 13, further comprising:

when the source address is not included in an entry of the cache, authorizing an acknowledgment signal for anticipatory transmission to the external source of the packet prior to retrieval of the key corresponding to the source address; and

MR2919-18
Serial Number: 09/662,991
Reply to Office Action dated 14 June 2006

when the source address is not included in an entry of the cache and

the source address is included in an entry of the system memory, using the key to

decrypt the body of the packet prior to arrival of a subsequent packet from the

external source.

16.   (Original) A method of key caching as claimed in claim 13, wherein

the cache includes fast memory.

17.   (Original) A method of key caching as claimed in claim 14, wherein

the cache includes fast memory.

18.   (Original) A method of key caching as claimed in claim 15, wherein

the cache includes fast memory.